## AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

**Listing of Claims:**

1. (currently amended) An apparatus comprising:

a first transistor disposed between a first node and an output node and having ~~a first control terminal~~ its gate coupled to receive a first dynamic data signal, wherein the first transistor is ~~coupled to a first node and is configured to drive a first state on the first node responsive to an assertion of the first dynamic data signal~~ inactive during a precharge phase, but is to be responsive to the first dynamic data signal during an evaluate phase to pull the output node towards a potential of the first node if a state of the first dynamic data signal activates the first transistor;

a second transistor disposed between the first node and the output node and having its gate coupled to ~~the first node and having a second control terminal, the second transistor configured to drive a second state on the first node responsive to a signal on the second control terminal~~ receive a second dynamic data signal, wherein the second transistor is inactive during the precharge phase, but is to be responsive to the second dynamic data signal during the evaluate phase to pull the output node towards the potential of the first node if a state of the second dynamic data signal activates the second transistor; and

~~a circuit coupled to generate the signal on the second control terminal and coupled to receive a second dynamic data signal, the second dynamic data signal being a complement of the first dynamic data signal, wherein the circuit is configured to activate the second transistor responsive to an assertion of the second dynamic data signal~~

a third transistor disposed between a second node and the output node and having its gate coupled to receive a NOR logic of complements of the first and second dynamic data signals, wherein the third transistor is inactive during the precharge phase, but is to be responsive to complements of the first and second dynamic data signals, in which if one of the first or second transistor is made active during the evaluate phase, the third transistor remains inactive, but if the first and second transistors are inactive during the

evaluate phase, the third transistor is made active to pull the output node towards a potential of the second node.

2. (currently amended) The apparatus as recited in claim 1 ~~further comprising a first plurality of transistors, wherein the first transistor is one of the first plurality of transistors and wherein the first dynamic data signal is one of a first plurality of dynamic data signals, each of the first plurality of transistors having a control terminal coupled to receive a respective one of the first plurality of dynamic data signals, wherein each of the first plurality of transistors is coupled to the first node and is configured to drive the first state on the first node responsive to an assertion of the respective one of the first plurality of dynamic data signals, and wherein the circuit is coupled to receive a second plurality of dynamic data signals including the second dynamic data signal, wherein each of the second plurality of dynamic data signals is a complement of a respective one of the first plurality of dynamic data signals, and wherein the circuit is configured to activate the second transistor responsive to an assertion of one of the second plurality of dynamic data signals~~ wherein the first and second transistors comprise two of a plurality of transistors disposed in parallel between the first node and the output node, the plurality of transistors having each respective gate coupled to receive a different dynamic data signal, wherein each of the plurality of transistors is inactive during the precharge phase, but is to be responsive to respective dynamic data signal during the evaluate phase to pull the output node towards a potential of the first node if a state of one of the different dynamic data signals activates one of the plurality of transistors; and the third transistor coupled to receive a NOR logic of complements of the different dynamic data signals, wherein the third transistor is inactive during the precharge phase, but is to be responsive to complements of the different dynamic data signals, in which if one of the plurality of transistors is made active during the evaluate phase, the third transistor remains inactive, but if the plurality of transistors remain inactive during the evaluate phase, the third transistor is made active to pull the output node towards a potential of the second node.

3. (currently amended) The apparatus as recited in claim ~~2~~ 1 wherein the ~~circuit performs a logical~~ NOR ~~of the second plurality of~~ logic of complements of the first and

second dynamic data signals is obtained by a NOR gate.

4. (currently amended) The apparatus as recited in claim ~~3~~ 2 wherein the ~~circuit is~~ NOR logic of complements of the different dynamic data signals is obtained by a NOR gate.

5. (canceled)

6. (currently amended) The apparatus as recited in claim ~~5~~ 1 wherein the ~~second transistor is a PMOS transistor~~ first and second transistors are NMOS transistors and the third transistor is a PMOS transistor.

7. (currently amended) The apparatus as recited in claim ~~6~~ 2 wherein the ~~second~~ plurality of transistors are each NMOS transistors and the third transistor is a PMOS transistor.

8. (canceled)

9. (currently amended) The apparatus as recited in claim ~~1~~ 6 further comprising an inverter ~~having an input coupled to the first node and driving an output signal representing the value represented by an asserted one of the first dynamic data signal or the second dynamic data signal~~ at the output node to generate an output having same logic state as the dynamic data signals.

10. (currently amended) The apparatus as recited in claim 1 further comprising a keeper coupled to the ~~first node and configured to retain a previous state of the first node responsive to a deassertion of each of the first dynamic data signal and the second dynamic data signal~~ output node to retain a state of the output node during a subsequent precharge phase.

11. (currently amended) The apparatus as recited in claim ~~10~~ 6 ~~wherein the~~ further comprising a keeper ~~is~~ coupled to ~~receive an indication of an evaluate phase of the first~~

~~and second dynamic data signals, and wherein the keeper is inactive during the evaluate phase~~ the output node to retain a state of the output node during a subsequent precharge phase.

12. (canceled)

13. (currently amended) A memory array comprising:

a plurality of banks of memory, each bank ~~configured~~ to output a ~~first~~ respective dynamic data signal indicative of a corresponding bit stored in the bank and a ~~second~~ complement of the dynamic data signal ~~indicative of the complement of the bit~~; and

a bank select circuit coupled to receive the ~~first~~ respective dynamic data signals and the ~~second dynamic data~~ complement signals from ~~each of~~ the plurality of banks and ~~configured~~ to output a ~~selected~~ global bit responsive to the ~~first~~ dynamic data signals ~~and the second dynamic data signal~~ from ~~each of~~ the plurality of banks, in which the bank select circuit ~~comprising~~ includes:

~~a first plurality of transistors, each having a control terminal coupled to receive the first dynamic data signal from a respective one of the plurality of banks, wherein each of the first plurality of transistors is coupled to a first node and is configured to drive a first state on the first node responsive to an assertion of the first dynamic data signal;~~

~~a second transistor coupled to the first node and having a second control terminal, the second transistor configured to drive a second state on the first node responsive to a signal on the second control terminal; and~~

~~a circuit coupled to generate the signal on the second terminal and coupled to receive the second dynamic data signal from each of the plurality of banks, wherein the circuit is configured to activate the second transistor responsive to an assertion of the second dynamic data signal from one of the plurality of banks~~

a plurality of transistors disposed in parallel between a first node and an output node, the plurality of transistors having each respective gate coupled to receive a different one of the respective dynamic data signals, wherein each of the plurality of transistors is inactive during a precharge phase, but is to be responsive

to respective dynamic data signal during an evaluate phase to pull the output node towards a potential of the first node if a state of one of the dynamic data signals activates one of the plurality of transistors during the evaluate phase; and

a common transistor coupled to receive a NOR logic of complements of the respective dynamic data signals, wherein the common transistor is inactive during the precharge phase, but is to be responsive to complements of the dynamic data signals during the evaluate phase, in which if one of the plurality of transistors is made active during the evaluate phase, the common transistor remains inactive, but if the plurality of transistors remain inactive during the evaluate phase, the common transistor is made active to pull the output node towards a potential of the second node.

14. (currently amended) The memory array as recited in claim 13 further comprising a decoder coupled to each of the plurality of banks, wherein the decoder is ~~configured~~ to ~~activate~~ select at most one of the plurality of banks to output ~~data via the first~~ its dynamic data signal ~~or the second dynamic data signal~~.

15. (currently amended) The memory array as recited in claim 13 wherein the bank select circuit further comprises an inverter ~~having an input coupled to the first node and a driving the selected bit output from the bank select circuit~~ at the output node to generate an output having same logic state as the dynamic data signals.

16. (currently amended) The memory array as recited in claim 13 wherein the bank select circuit further comprises a keeper coupled to the ~~first~~ output node ~~and configured~~ to retain a ~~previous~~ state of the ~~first~~ output node ~~responsive to a deassertion of each of first dynamic data signals and the second dynamic data signals~~ during a subsequent precharge phase.

17. (currently amended) The memory array as recited in claim 13 wherein the ~~circuit performs a logical~~ NOR ~~of the second dynamic data signals from each of the plurality of banks~~ logic of complements of the dynamic data signals is obtained by a NOR gate.

18-19. (canceled)

20. (currently amended) The memory array as recited in claim ~~19~~ 13 wherein the ~~second transistor is~~ plurality of transistors are NMOS transistors and the common transistor is a PMOS transistor.

21. (currently amended) The memory array as recited in claim 20 wherein ~~the second plurality of transistors are each NMOS transistors~~ the potential of the second node is a supply voltage potential and the potential of the first node is a supply return potential.

22. (canceled)

23. (currently amended) A computer accessible medium comprising one or more data structures representing:

~~a first plurality of transistors, each having a control terminal coupled to receive a respective one of a first plurality of dynamic data signals, wherein each of the first plurality of transistors is coupled to a first node and is configured to drive a first state on the first node responsive to an assertion of the respective one of the first plurality of dynamic data signals;~~

~~a second transistor coupled to the first node and having a second control terminal, the second transistor configured to drive a second state on the first node responsive to a signal on the second control terminal; and~~

~~a circuit coupled to generate the signal on the second terminal and coupled to receive a second plurality of dynamic data signals, each of the second plurality of dynamic data signals being a complement of a respective one of the first plurality of dynamic data signals, wherein the circuit is configured to activate the second transistor responsive to an assertion of one of the second plurality of dynamic data signals~~

a plurality of transistors disposed in parallel between a first node and an output node, the plurality of transistors having each respective gate coupled to receive a different one of dynamic data signals, wherein each of the plurality of transistors is inactive during

a precharge phase, but is to be responsive to respective dynamic data signal during an evaluate phase to pull the output node towards a potential of the first node if a state of one of the dynamic data signals activates one of the plurality of transistors during the evaluate phase; and

a common transistor coupled to receive a NOR logic of complements of the respective dynamic data signals, wherein the common transistor is inactive during the precharge phase, but is to be responsive to complements of the dynamic data signals during the evaluate phase, in which if one of the plurality of transistors is made active during the evaluate phase, the common transistor remains inactive, but if the plurality of transistors remain inactive during the evaluate phase, the common transistor is made active to pull the output node towards a potential of the second node..

24. (currently amended) The computer accessible medium as recited in claim 23 wherein the one or more data structures further represent a memory array, the memory array comprising:

a plurality of banks of memory, each bank ~~configured~~ to output a ~~first~~ respective dynamic data signal indicative of a corresponding bit stored in the bank and a ~~second~~ complement of the dynamic data ~~signal indicative of the complement of the bit~~; and

a bank select circuit coupled to receive the ~~first~~ respective dynamic data signals and the ~~second dynamic data~~ complement signals from ~~each of~~ the plurality of banks and ~~configured~~ to output a ~~selected~~ global bit responsive to the ~~first~~ dynamic data signals ~~and the second dynamic data signal~~ from ~~each of~~ the plurality of banks, in which the bank select circuit ~~comprising~~ the ~~first~~ plurality of transistors~~,~~ and the ~~second~~ common transistor~~, and the circuit~~.

25. (currently amended) A computer accessible medium comprising one or more data structures representing:

a first transistor disposed between a first node and an output node and having ~~a first control terminal~~ its gate coupled to receive a first dynamic data signal, wherein the first transistor is ~~coupled to a first node and is configured to drive a first state on the first node responsive to an assertion of the first dynamic data signal~~ inactive during a

precharge phase, but is to be responsive to the first dynamic data signal during an evaluate phase to pull the output node towards a potential of the first node if a state of the first dynamic data signal activates the first transistor;

a second transistor disposed between the first node and the output node and having its gate coupled to ~~the first node and having a second control terminal, the second transistor configured to drive a second state on the first node responsive to a signal on the second control terminal~~ receive a second dynamic data signal, wherein the second transistor is inactive during the precharge phase, but is to be responsive to the second dynamic data signal during the evaluate phase to pull the output node towards the potential of the first node if a state of the second dynamic data signal activates the second transistor; and

~~a circuit coupled to generate the signal on the second control terminal and coupled to receive a second dynamic data signal, the second dynamic data signal being a complement of the first dynamic data signal, wherein the circuit is configured to activate the second transistor responsive to an assertion of the second dynamic data signal~~

a third transistor disposed between a second node and the output node and having its gate coupled to receive a NOR logic of complements of the first and second dynamic data signals, wherein the third transistor is inactive during the precharge phase, but is to be responsive to complements of the first and second dynamic data signals, in which if one of the first or second transistor is made active during the evaluate phase, the third transistor remains inactive, but if the first and second transistors are inactive during the evaluate phase, the third transistor is made active to pull the output node towards a potential of the second node.